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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/790,852
Filing Date: March 02, 2004
Appellant(s): WIECZOREK ET AL.

J. Mike Amerson
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 11/15/05 appealing from the Office action mailed 06/02/2005.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,252,277 B1	CHAN ET AL.	6-2001
6,355,955 B1	GARDNER ET AL.	3-2002

Applicant's admitted prior art (Figures 1a-1d and pages 1-8 of the instant specification)

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4, 9-15, 21-23 and 25-31 are rejected under 35 U.S.C. 102(b) as being anticipated by Chan et al. (U.S. Patent No. 6,252,277). With regard to Claim 1, Chan discloses a method of forming a field effect transistor, the method comprising:

forming an implantation mask (37) over a crystalline semiconductor region (30) (figure 4C);

forming drain and source regions (39) adjacent said implantation mask (37) (figure 4E), said drain and source regions (39) each having a top surface located above a top surface of said crystalline semiconductor region (30) (figure 4E);

removing said implantation mask (37) to expose a top surface area of said crystalline semiconductor region (30);

forming a gate insulation layer (44) on said exposed surface area (column 5, lines 57-59);

forming a gate electrode (47), out of polysilicon layer (46), on said gate insulation layer (44); and

doping said gate electrode (column 5, lines 61-67 and column 6, lines 1-7).

With regard to Claim 2, Chan discloses forming a gate electrode (47) including depositing a gate electrode material (46) comprising polysilicon (column 5, lines 61-63) above a gate insulation layer (44) and removing excess material of said gate electrode material (46) to form the gate electrode (47) (column 6, lines 8-9 and figure 4I).

With regard to Claim 3, Chan discloses a lateral size of the implantation mask (37) that is greater than a design value of a gate length of the gate electrode (47), as clearly seen on figures 4B, 4F and 4I, wherein the implantation mask (37) occupies a lateral size that is larger than that which is occupied by gate electrode (47) as part of the final structure disclosed by the reference.

With regard to Claim 4, Chan discloses forming drain and source regions (39) by epitaxially-growing (column 5, lines 7-17) a crystalline semiconductor layer adjacent to an implantation mask (37).

With regard to Claim 9, Chan discloses forming sidewall spacers (35) on sidewalls of the drain and source regions (column 5, lines 10-13) that are exposed by removing an implantation mask (37).

With regard to Claim 10, Chan discloses a width of sidewalls spacers (35) controlled on the basis of target length (figure 4B) for a gate electrode (47).

With regard to Claim 11, Chan discloses an implantation mask (37) that is removed by an isotropic-etch process (column 5, lines 51-54).

With regard to Claim 12, Chan discloses removing an excess material (46) to form a gate electrode (47), by chemical-mechanical polishing (column 6, lines 8-9).

With regard to Claim 13, Chan discloses removing an excess material (46) to form a gate electrode (47), by an etch-process (column 6, lines 9-10).

With regard to Claim 14, Chan discloses removing an excess material (46) to form a gate electrode (47), by chemical-mechanical polishing (column 6, lines 8-9) and an etch-process (column 6, lines 9-10).

With regard to Claim 15, Chan discloses forming metal/semiconductor compound regions (48A, 48B) (column 6, lines 29-39) on the gate electrode (47) and drain and source regions (39).

With regard to Claim 21, Chan discloses doping of the gate electrode (47) that is performed on the basis of process parameters selected to restrict dopant-penetration of the gate insulation layer (column 5, lines 57-67 and column 6, lines 1-3).

With regard to Claim 22, Chan discloses a field-effect transistor (column, lines 4-6), comprising:
a substrate (30) having formed thereon a semiconductor region having a top surface; a drain region (39) formed on said top surface of said semiconductor region and extending along a lateral direction and a height direction (figure 4E); a source region (39) formed on said top surface of said semiconductor region and extending along a lateral direction and a height direction (figure 4E); a gate electrode (47)) formed above said top surface of said semiconductor region and extending along said lateral direction and said height direction said gate electrode (47) laterally located between said drain and source regions (39) and separated from said top semiconductor region by a gate

insulation layer (44), said drain and source regions (39) extending along said height direction at least to an upper surface of said gate electrode (47) (figure 4E).

With regard to Claim 23, Chan discloses a gate electrode (47) that is partially-comprised of a doped semiconductor material (column 5, lines 67-68 and column 6, lines 1-3); whereby a peak concentration of dopants in said gate electrode is less than a peak concentration of dopants in said drain and source regions (39), since said drain and source regions (39) are heavily-doped (column 5, lines 13-15).

With regard to Claim 25, Chan discloses a method of forming a field effect transistor (column, lines 4-6), the method comprising:

forming a recess (136) in a semiconductor layer (30), said recess having a bottom surface; forming an implantation mask (137) in at least said recess (136);

forming drain and source regions (139) by performing at least one ion implantation to implant ions (arsenic) into said semiconductor layer (30) adjacent said implantation mask, wherein said implantation mask (137) substantially prevents ions from penetrating said bottom surface of said recess (136);

removing said implantation mask to expose said bottom surface of said recess (136) (column 8, lines 57-60);

forming a gate insulation layer (144) on said exposed surface area (column 8, lines 64-67);

forming a gate electrode (147), out of polysilicon layer (146), on said gate insulation layer (144) (column 9, lines 1-25); and

doping said gate electrode (column 9, lines 4-14).

With regard to Claim 26, Chan discloses forming a gate electrode (47) including depositing a gate electrode material comprising polysilicon (column 5, lines 61-63) above a gate insulation layer (44) and removing excess material of said gate electrode to form the gate electrode (column 6, lines 8-12 and figure 4I).

With regard to Claim 27, Chan discloses forming sidewall spacers (135), prior to forming the gate insulation layer (144), on sidewalls of the recess (136) that are exposed by removing an implantation mask (137).

With regard to Claim 28, Chan discloses a width of sidewalls spacers (135) controlled on the basis of target length (figure 6B) for a gate electrode (147).

With regard to Claim 29, Chan discloses an implantation mask (37) that is removed by an isotropic-etch process (column 5, lines 51-54).

With regard to Claim 30, Chan discloses forming metal/semiconductor compound regions (148A, 148B) (column 6, lines 29-39) on the gate electrode (47) and drain and source regions (39).

With regard to Claim 31, Chan discloses a lateral dimension of a recess (136) that is greater than a target length of a gate electrode (47), (figures 4B and 4I).

With regard to Claim 32, Chan discloses a recess (136) formed by anisotropically etching the semiconductor layer (30) (column 7, lines 44-50).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chan et al. (U.S. Patent No. 6,252,277) in view of Applicant's admitted prior art as disclosed on pages 1-8 and figures 1a-1d of the instant application. With regard to Claim 5, Chan essentially discloses the claimed invention but fails to disclose the claimed steps of a first implantation sequence for drain and source regions is performed prior to epitaxially-growing the semiconductor layer and a second implantation sequence for forming said drain and source regions is performed after epitaxially-growing the semiconductor layer. However, Applicant's admitted prior art discloses a process for forming a transistor which includes the steps of a first implantation sequence for drain and source regions (108) (see page 5, lines 21-24 of the instant application) that is performed prior to epitaxially-growing silicon regions (111) (see page 7, lines 11-12 of the instant

application), wherein the epitaxially-growing silicon regions (111) may be grown prior to or after a final implantation cycle for forming the drain and source regions (108) (see page 7, lines 13-15 of the instant application). Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the process as disclosed by Chan to include the claimed steps of a first implantation sequence for drain and source regions is performed prior to epitaxially growing the semiconductor layer and a second implantation sequence for forming said drain and source regions is performed after epitaxially growing the semiconductor layer, as clearly suggested by Applicant's admitted prior art, in order to reduce contact resistance to the drain and source regions (see page 7, lines 1-9 of the instant application).

With regard to Claim 6, a further difference between the claimed invention and Chan is the claimed step of an anneal process to activate the dopants. However, Applicant's admitted prior art discloses a process for forming a transistor, which includes the step of using an anneal process to activate dopants on drain and source regions (108) (see page 5, lines 21-24 and page 6, lines 3-5 of the instant application). Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the process as disclosed by Chan to include the claimed step of an anneal process to activate the dopants, as clearly suggested by Applicant's admitted prior art, in order to activate dopants and re-crystallize portions of drain and source regions that are damaged during implantation sequences (see page 6, lines 3-5 of the instant application).

With regard to Claim 7, a further difference between the claimed invention and Chan is the claimed anneal process controlled on the basis of a desired channel length defined by a lateral distance of the drain region and the source region. However, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the process as disclosed by Chan to include the claimed anneal process controlled on the basis of a desired channel length defined by a lateral distance of the drain region and the source region, in order to optimize the channel-length and thus reduce problems associated with a channel region, namely leakage current.

With regard to Claim 8, a further difference between the claimed invention and Chan is the claimed step of an anneal cycle performed after said first implantation sequence and prior to said second implantation sequence, said first anneal cycle being configured to substantially completely re-crystallize amorphized portions in said semiconductor region. However, Applicant's admitted prior art discloses a process for forming a transistor, which includes the step of using an anneal process to activate dopants and re-crystallize portions of drain and source regions (108) that are damaged by previous implantation sequences (see page 5, lines 21-24 and page 6, lines 3-5 of the instant application). Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the process as disclosed by Chan to include the claimed step of an anneal process to activate the dopants, as clearly suggested by Applicant's admitted prior art, in order to activate dopants and re-crystallize portions of

drain and source regions that are damaged during implantation sequences (see page 6, lines 3-5 of the instant application).

Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chan et al. (U.S. Patent No. 6,252,277) in view of Gardner (U.S. Patent No. 6,355,955). With regard to Claim 24, Chan essentially discloses the claimed invention but fails to disclose the claimed semiconductor region formed on an insulating layer and having an extension in the height direction in the range of approximately 5-50 nm. However, Gardner discloses that the height of a semiconductor layer can be modified as desired (column 12, lines 36-54). Therefore it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the method as disclosed by Chan to include the claimed height, in order to minimize diffusion of impurities into the channel region (column 12, lines 50-54). Additionally, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233. Regarding the claimed insulating layer, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the method as disclosed by Chan to include a semiconductor region formed on an insulating layer, in order to provide an insulating layer for semiconductor device such as a thin-film transistor (TFT).

(10) Response to Arguments

Claims 1-4, 9-15 and 21

Appellant's arguments in regard to claims 1-4, 9-15 and 21 are directed towards limitations recited in claim 1. Appellant presents no separate arguments with regard to claims 2-4, 9-15 and 21, all of which depend from claim 1.

With regard to claim 1, appellant's arguments center on two basic points.

First, that the source and drains of Chan et al. are not formed adjacent the implantation mask. This first argument will be addressed below by the Examiner by addressing the proper interpretation of the term "adjacent" and the interpretation of the Chan et al. reference.

Second, that the implantation mask is not removed to expose a top surface of the crystalline semiconductor region and that the gate insulation layer is formed on the exposed surface of the top surface of the crystalline semiconductor region. This second argument will be addressed below by the Examiner by addressing the proper interpretation of the term "top surface" as well as which surface is defined by the claimed crystalline semiconductor region.

First, appellant argues that the source and drains of Chan et al. are not formed adjacent the implantation mask. This argument is not persuasive. It is noted that the term "adjacent" does not require physical contact between two structures, merely that

they are in close proximity. Thus, as seen in figures 4D and 4E of Chan et al., the source/drain regions 39 are formed "adjacent" to the implantation mask 37. The existence of spacer 35 between the source/drain regions 39 and the implantation mask 37 does not preclude 37 and 39 from being "adjacent" each other. Appellant is arguing an improperly narrow interpretation for the language of their claims. Appellant apparently feels that the term "adjacent" should be narrowly interpreted so as to require the structures be abutting each other with no offset therebetween. This narrow interpretation of the claim language is not proper. Appellant's specification does not specifically define the term "adjacent" or provide any clear guidance as to how the term should be interpreted or why it should be interpreted in a narrower manner than it's accepted meaning. Thus, following the doctrine of giving claimed terminology it's broadest reasonable interpretation, "adjacent" has been interpreted to mean "in close proximity" and not necessarily contacting or abutting with no offset. Using this reasonable interpretation of the term "adjacent", it can clearly be seen in figure 4E of Chan et al. that the source/drain regions 39 are formed "adjacent" to the implantation mask 37, thus meeting the language of the claim.

Further, even if for arguments sake we give "adjacent" the improperly narrow interpretation that appellant argues, Chan et al. still discloses the source/drain regions adjacent to the implantation mask. Claim 1 recites "forming an implantation mask over a crystalline semiconductor region." Layers 35 and 37 of Chan et al., taken together, can properly be considered the implantation mask (see figure 4D). Thus, when the source/drain regions 39 are formed in figure 4E, they are formed adjacent to the

implantation mask 35/37. Using this reasonable interpretation of Chan et al., the limitation at issue is disclosed regardless of whether the narrower or broader interpretation is lent to "adjacent."

Second, appellant argues that the implantation mask is not removed to expose a top surface of the crystalline semiconductor region and that the gate insulation layer is formed on the exposed surface of the top surface of the crystalline semiconductor region. This argument is not persuasive. It is noted that the term "top surface" is not properly limited to merely the surface at the highest point or highest elevation of the structure. The "top surface" can include the entire surface on the upper side of the layer, including any topology formed therein. As an analogy, when considering what constitutes the top surface of a car, one would include the upper surface of the hood and trunk, not merely the more elevated upper surface of the passenger area. Using this common interpretation of "top surface", the top surface of the crystalline semiconductor region of Chan et al. is exposed by removing the implantation mask 37 and a gate insulation film 44 is formed on this exposed "top surface" (see figure 4G of Chan et al.). Appellant is arguing an improperly narrow interpretation for the language of their claims. Appellant apparently feels that the term "top surface" should be so narrowly interpreted so as to define only a surface at it's highest elevation (i.e. precluding sections of the surface that may be lower due to the topography of the structure). This narrow interpretation of the claim language is not proper. Appellant's specification does not explicitly, or even implicitly, define the term "top surface" or

provide any clear guidance as to how the term should be interpreted or why it should be interpreted in a narrowed manner than it's accepted meaning. Giving the term "top surface" it's broadest reasonable interpretation, "top surface" has been properly interpreted to mean the entire upper surface of the layer, including those portions of the upper surface that are lower in elevation along the topography of the structure. Using this interpretation, it is easily understood that the bottom of the trench is still a part of the "top surface" (see figure 4B of Chan et al.).

Further, the limitation at issue limits the "top surface" to the "crystalline semiconductor region." This "crystalline semiconductor region" can be interpreted in two ways. First, if the "crystalline semiconductor region" is considered to be the entire substrate 30 as shown in figure 4A, then the "top surface" when the implantation mask is formed will be the entire upper topography in figure 4B including the original upper surface (the interface between layer 32 and substrate 30 as well as between layer 35 and substrate 30) as well as the surfaces in the trench. Thus, even the surface of the substrate in the bottom of the trench is part of the "top surface of the crystalline semiconductor region." Alternatively, since the "crystalline semiconductor region" is not defined in the claim except as that which the implantation mask is formed upon, the "crystalline semiconductor region" can be considered merely the portion of the substrate 30 that the implantation mask 37 is formed upon (that is the portion of substrate 30 underneath the trench 46 and laterally bounded by the trench sidewalls). In this case, the only reasonable "top surface" of this region is the surface at the bottom of the trench.

Regardless of which reasoning is followed for interpreting "top surface", the surface at the bottom of the trench as seen in figure 4B of Chan et al. is properly interpreted as part of the top surface. Thus, as clearly seen in figure 4G, the implantation mask 37 is removed to expose "a top surface area of said top surface of said crystalline semiconductor region" and a gate insulation layer 44 is formed on this exposed top surface area of the top surface of the crystalline semiconductor region.

Keeping the above discussion of "adjacent" and "top surface" in mind, appellant's more specific arguments with regard to claim 1 are not persuasive as explained below.

Appellant argues that it is unclear where in Chan et al. the examiner finds support for the assertion that the epitaxial silicon regions 39 are formed adjacent the implantation mask 37 that remains positioned in the trench 36. Appellant argues that since the source/drain regions 39 of Chan et al. are offset from the implantation mask by the width of spacers 35, the source/drain regions 39 are not formed adjacent the implantation mask. This is not persuasive since the claimed limitation is clearly shown in figure 4E of Chan et al. If "adjacent" is given it's broadest reasonable interpretation, regions 39 are "adjacent" to the mask 37 in that they are in close proximity to the mask. Alternatively, if the implantation mask is considered to include both layers 35 and 37, regions 39 are clearly seen as being "adjacent" to the mask 35/37 regardless of whether the narrower or broader meaning is lent to adjacent. Stated another way, the existence of the spacers 35 do not preclude the source/drain regions 39 from still being "adjacent"

to the implantation mask since: either adjacent can be properly interpreted as not requiring contact but merely close proximity; or the spacers 35 can be considered as part of the implantation mask.

Appellant then argues that Chan et al. does not teach removing the implantation mask to expose a surface area of a top surface of the crystalline semiconductor region, and forming a gate insulation layer on the exposed surface of the top surface of the crystalline semiconductor region since in Chan et al. the gate oxide 44 is formed on the exposed silicon surface within the trench, i.e. on the bottom of the trench. This is not persuasive since, as explained above, the "a surface area of a top surface of the crystalline semiconductor region" includes the surface of the trench, i.e. the bottom of the trench. Since the bottom of the trench reads on the claimed "a surface area of the top surface of the crystalline semiconductor region", it is clearly seen in figures 4E-4G where the implantation mask is removed to expose this area and a gate insulation film 44 is formed on this exposed area.

Appellant furthers this argument by stating that equating the bottom surface of the trench with the top surface of the semiconductor region is (1) contrary to the teachings set forth in the specification of the present application and (2) contrary to what one skilled in the art would understand the top surface of the semiconductor region to be. This is not persuasive. First, appellant has not pointed out where these "teachings" are found in the specification of the present application and upon reviewing the

specification the Examiner cannot locate any teachings that a bottom surface of a trench cannot be considered part of a top surface of the semiconductor region. Second, appellant has provided no evidence as to why one skilled in the art would not understand the "top surface of the semiconductor region" to include the bottom of the trench. As explained above, the "semiconductor region" can properly be limited to only that portion of the substrate 30 of Chan et al. that is directly beneath and laterally bounded by the trench. As such, the bottom surface of the trench is properly equated with the claimed top surface. Appellant also argues that to construe the bottom of the trench to be a top surface would be inconsistent with a specifically disclosed embodiment in the specification. This is not persuasive as it is not proper to read limitations and entire embodiments from the specification into the claims. The fact that Chan et al. discloses the claimed invention points to the fact that the claims, as written, are broader in scope than the specific embodiment disclosed in appellant's specification.

Appellant also argues that since the starting material 30 of Chan et al. has a planar top surface, the bottom surface of a trench formed in the wafer 30 would not be understood to be a "top surface" of that wafer. First, the claims do not recite a "top surface of that (the starting) wafer." As such, this point of the argument does not point out how the claimed invention is different than that of Chan et al. Second, the claims do not require the "top surface" be the same top surface as a starting wafer. The claims do not preclude other processing steps having occurred such as the trench formation. The

claims merely refer to a "top surface" of a "crystalline semiconductor region" that has an implantation mask formed thereon, regardless of what other steps may have occurred to the starting wafer.

Claims 25-32

Appellant's arguments in regard to claims 25-32 are directed towards limitations recited in claim 25. Appellant presents no separate arguments with regard to claims 26-32, all of which depend from claim 25.

Appellant argues that Chan et al. does not disclose the limitation of performing an ion implant process to form source/drain regions by implanting ions adjacent the implantation mask. This is not persuasive. First, it is noted that the rejection relies upon the embodiment shown in figures 6A-6I for the rejection of these claims where previously the rejection relied upon the embodiment shown in figures 4A-4K. As seen in figure 6E, an ion implant process is performed to form source/drain regions 139. The examiner's position with regard to the limitation "adjacent" as explained above applies to these claims as well. As explained above, "adjacent" merely required close proximity such that the ion implant process of Chan et al. forms source/drain regions 139 "adjacent" to the implantation mask 137. Alternatively, as explained above, spacers 135 can be considered part of the implantation mask such that the source/drain regions 139 are formed "adjacent" to the implantation mask 135/137.

Claims 22-24

Appellant's arguments in regard to claims 22-24 are directed towards limitations recited in claim 22. Appellant presents no separate arguments with regard to claims 23 and 24, which depend from claim 22.

Appellant argues that Chan et al. do not teach the gate electrode 47 formed above a top surface of the semiconductor region nor is it separated from the top surface of the semiconductor region by a gate insulation layer. This is not persuasive. As explained above, the "top surface" of the semiconductor region is not properly limited to solely the highest portion of the surface, or to the top surface of the original starting wafer. The "top surface" is properly interpreted to include the surfaces along the trench, including the bottom of the trench. Thus, as clearly seen in figure 5 of Chan et al., for example, the gate electrode 47 (labelled 46 in figure 5, see figure 4J for example for the same structure being labelled 46 and 47) is formed above a top surface and separated from the top surface by gate insulation layer 44.

Claims 5-8

Appellant's arguments with regard to claim 5-8 are not persuasive. Appellant argues that Chan et al. teaches away from the method recited in claim 5. This is not persuasive. The fact that Chan et al. teaches a different method than that claimed does not mean that Chan et al. teaches away from the proposed modification to achieve the method claimed. Chan et al. does not contain any language that explicitly teaches that their method cannot be combined with a different method.

Appellant also argues that the examiner "magically concludes" that it would have been obvious to arrive at the invention based upon a combination of Chan et al. with Appellant's admitted prior art. This argument is not persuasive as the examiner did not "magically conclude" the obviousness of the combination. The examiner concluded that it would have been obvious to combine Chan et al. with appellant's admitted prior art based upon clearly stated motivation provided in the rejection. The rejection even pointed out that the motivation came directly from the references themselves such that the motivation is from the record and not a "magical" conclusion.

Appellant furthers these arguments by stating that the examiner does not provide any (emphasis added) reason why one skilled in the art would be motivated to ignore the express teachings of Chan and perform additional implantation steps. Appellant argues that such additional steps would be time consuming and expensive and as such one of ordinary skill in the art would not be motivated to modify the teachings of Chan so as to arrive at appellant's invention. This argument is not persuasive as the rejection clearly sets out particular motivation for including the extra processing steps and thus properly teaches why one of ordinary skill in the art would be motivated to modify the teachings of Chan et al. so as to arrive at the claimed invention. As recited in the rejection of claim 5, it would have been obvious to modify the process of Chan et al. "in order to reduce contact resistance to the drain and source regions" (see the last three lines of the rejection of claim 5 on page 8 of the final Office Action mailed 6/14/05, reproduced on the lines spanning pages 9 and 10 of this Examiner's Answer). Thus,

the examiner did provide adequate reasoning, from the prior art itself, as to why one of ordinary skill in the art would be motivated to perform the proposed modification of Chan et al. to arrive at the claimed invention.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

N. Drew Richards

Conferees:

Ken Parker

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